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re Patent Application of:

Shmuel Ur, et al.

: Confirmation No.: 3388

Serial No.: 10/699,227

: Group Art Unit: 2857

Filed: October 31, 2003

: Examiner:

For: Late binding of variables during test case generation for hardware and software design verification

: Date: March 10, 2005

**INFORMATION DISCLOSURE STATEMENT
under 37 C.F.R. 1.97(b)(3)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on form PTO-1449 are a number of documents which may be material to the examination of the above-referenced application. It is respectfully requested that the Examiner consider each of the cited documents and return an initialed copy of the form PTO-1449.

In accordance with 37 CFR 1.97(b), this information disclosure statement is being filed within three months of the filing date of the application or before the mailing date of the first Office Action on the merits, which ever event occurs last. **Please charge any fee necessary to enter this paper to deposit account 09-0468.**

Respectfully submitted,
Attorney for the Applicant(s)

By Stephen C. Kaufman
Registration No.: 29,551

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IBM Docket: IL920030044US1



FORM PTO-1449 (Modified)

**LIST OF PATENTS AND PUBLICATIONS
FOR APPLICANT'S INFORMATION
DISCLOSURE STATEMENT**

ATTY. DOCKET NO.

IL920030044US1

SERIAL NO.:

10/699,227

APPLICANT:

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FILING DATE:

October 31, 2003

GROUP: 2857

REFERENCE DESIGNATION**U.S. PATENT DOCUMENTS**

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
AA						

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
AB							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

AC	Lichtenstein, Yossi et al., "Model Based Test Generation for Processor Verification", Sixth Innovative Applications of Artificial Intelligence Conference, August 1994, pp. 83-94.
AD	Chandra, A. et al., "AVPGEN - A Test Generator for Architecture Verification", IEEE Trans. on Very Large Scale Integration (VLSI) Systems, Vol. 3, No. 2, pp. 188-200 (June 1995).
AE	O'Kafka, Brian et al., "MPTG: A Portable Test Generator for Cache-Coherent Multiprocessors", International Conference on Computers and Communicatins, 1995 IEEE, pp. 38-44.
AF	Bergmann, Jules et al., "Improving Coverage Analysis and Test Generation for Large Designs". Proceedings of the International Conference on Computer Design, pp. 580-583, Nov. 1999.
AG	Seger, C.J. et al., "Formal Verification by Symbolic Evaluation of Partially-Ordered Trajectories" Formal Methods in System Design: An International Journal, 6(2): 147-189, March 1995.
AH	Edelstein, O., et al., "Multithreaded Java Program Test Generation", IBM Systems Journal, Vol. 41, No. 1, 2002, pp. 111-125.
AI	Stoller, S. et al., "Model-Checking Multi-Threaded Distributed Java Programs", Proceedings of the 7th International SPIN Workshop on Model Checking of Software, pp. 224-244, New York, 2000.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shmuel Ur, et al.

Docket No.: IL920030044US1

Serial No.: 10/699,227

Examiner:

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Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)

I hereby certify that the attached correspondence comprising:

1. Information Disclosure Statement Transmittal Letter;
2. PTO Form 1449 with 7 references attached
3. Return Postcard

is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on March 10, 2005.

Jeanne M. Jordan

(Type or print name of person mailing paper)

Jeanne M. Jordan

(Signature of person mailing paper)